**Amendments To The Drawings**

No amendments have been made to the drawings.

## REMARKS

Claims 20-39 are pending. The Office Action dated February 23, 2006, in this Application has been carefully considered. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. In this response, claims 1-19 have been canceled, and claims 20-39 have been added. Reconsideration and allowance are respectfully requested in light of the above amendments and the following remarks.

In the Office Action, the Examiner objected to claim 8 due to a typographical error. In response thereto, Applicant notes that claim 8 has been canceled.

In the Office Action, the Examiner advised that should claims 12 and 14 be found allowable, claim 14 would be objected to as being a substantial duplicate of claim 12. In response thereto, Applicant notes that claims 12 and 14 have been canceled.

Claims 1-11, 13, and 15 were rejected under 35 U.S.C. 102(e) as being anticipated by Pessolano (U.S. Patent Application Publication 2004/0268091). In response thereto, Applicant notes that claims 1-11, 13, and 15 are canceled herein.

Pessolano discloses a processor having multiple execution units and multiple registers for storing instructions for execution by the execution units. The registers are coupled to the execution units via a distribution means having multiple dispatch units coupled to the execution units, and a data communication bus coupling the execution units to the dispatch units. The data communication bus is controlled by a control unit. The dispatch units are arranged to detect dedicated instructions in the instruction flow that signal the beginning of an inactive period of an execution unit. Subsequently, the control unit is notified, and the instruction flow from the registers to the dispatch units is rerouted as a result of the detection of the dedicated instruction.

Applicant notes that Pessolano does not teach or disclose a method for reducing electrical power dissipation in a computer system including: providing a counter corresponding to a data channel, and a processor coupled to receive computer program instructions and configured to execute the received computer program instructions; determining at least one component of the processor that is not used when the processor has executed all received computer program instructions and is waiting for further computer program instructions; decrementing a count stored in the counter when the processor executes an instruction corresponding to the data channel; and transitioning the at least one component of the processor to a low power mode in the event the count stored in the counter reaches a predetermined value.

Applicant also notes that Pessolano does not describe a computer system including: a counter corresponding to a data channel; a processor coupled to receive computer program instructions and a power control signal, wherein the processor is configured to execute the received computer program instructions, and wherein the processor comprises at least one component that is not used when the processor has executed all received computer program instructions and is waiting for further computer program instructions, and wherein the processor is configured to transition the at least one component to a low power mode in response to the power control signal; means for decrementing a count stored in the counter when the processor executes an instruction corresponding to the data channel; and means for producing the power control signal in the event the count stored in the counter reaches a predetermined value.

Applicant believes that pending claims 20-39 are allowable in view of Pessolano.

Claims 12, 14, and 16-19 were rejected under 35 U.S.C. 102(e) as being anticipated by Filippo (U.S. Patent No. 6,983,389). In response thereto, Applicant notes that claims 12, 14, and 16-19 are canceled herein.

Filippo discloses an integrated device including multiple functional units and an activity detector and clock control unit corresponding to each of the functional units. Each activity detector and clock control unit is configured to monitor input signals received by, and output signals produced by, the corresponding functional unit to predict when the functional unit will be inactive. Each activity detector and clock control unit is configured to provide a clock signal to the corresponding functional unit when active, and to shut off the clock signal to the corresponding functional unit in response to predicted inactivity of the functional unit.

Applicant notes that Filippo does not teach or disclose a method for reducing electrical power dissipation in a computer system including: providing a counter corresponding to a data channel, and a processor coupled to receive computer program instructions and configured to execute the received computer program instructions; determining at least one component of the processor that is not used when the processor has executed all received computer program instructions and is waiting for further computer program instructions; decrementing a count stored in the counter when the processor executes an instruction corresponding to the data channel; and transitioning the at least one component of the processor to a low power mode in the event the count stored in the counter reaches a predetermined value.

Applicant also notes that Filippo does not describe a computer system including: a counter corresponding to a data channel; a processor coupled to receive computer program instructions and a power control signal, wherein the processor is configured to execute the received computer program instructions, and wherein the processor comprises at least one component that is not used when the processor has executed all received computer program instructions and is waiting for further computer program instructions, and wherein the processor is configured to transition the at least one component to a low power mode in response to the power control signal; means for

decrementing a count stored in the counter when the processor executes an instruction corresponding to the data channel; and means for producing the power control signal in the event the count stored in the counter reaches a predetermined value.

Applicant believes that pending claims 20-39 are allowable in view of Filippo.

In the present response, Applicant addresses all of the claim objections and rejections cited in the Office Action. In view of the amendments to the claims and Applicant's remarks, Applicant believes pending claims 20-39 in condition for allowance, and respectfully request allowance of pending claims 20-39.

With the amendments to the claims presented herein, there are currently 4 pending independent claims and 20 total pending claims in the application. As the original application had 9 independent claims and 19 total claims, Applicant believes no additional fees are due. In the event that any other fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

The present amendment is believed to contain a complete response to the issues raised in the Office Action. Full reconsideration is respectfully requested. If the Examiner should have any questions, comments or suggestions, the undersigned attorney earnestly requests a telephone conference. In particular, should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is also invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

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